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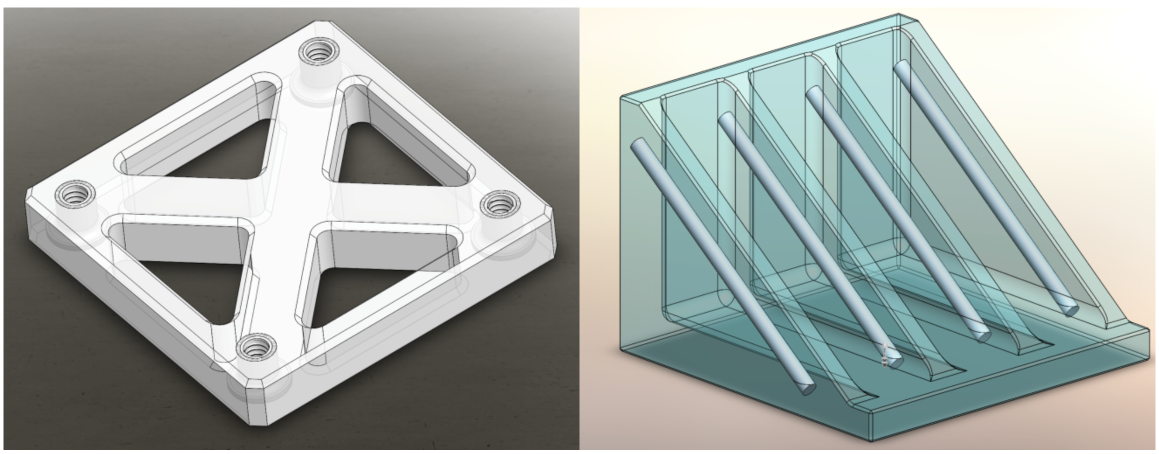
PCB Conceptual Design



TEAM F

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Requirements Formulation

Because Team F's project does not require construction or modification of a power distribution system, we have instead elected to develop a digital transceiver board for sending temperature readings across a mechanical slip ring. Mechanical slip rings can introduce significant noise to signal transmissions and thus we have deemed it desirable to create a small form factor board which can convert the high impedance analog thermistor signal to a more noise-tolerant digital signal. Because the board will need to be mounted to the extruder nozzle of our 3D printer, small form factor is an important design consideration. Also, since all power and data lines will require a dedicated channel in the slip ring, minimizing the number of required lines is highly desirable. Finally, since the temperature signal will need to be sent to the 3D printer's original control board, utilizing a communication protocol which is already available on the GPIO pins of the original controller will simplify the overall integration. This produces the following requirements for the transceiver board.

1. Small form factor
2. Tolerant to slip-ring induced noise in power lines
3. Minimum 1 channel ADC, ideally more to optionally provide redundant thermistors
4. Digital serial output that is robust to slip-ring induced noise
5. Serial digital output which is compatible with serial protocols already available on Rambo control board
6. Parts are affordable and obtainable

These requirements are implemented as follows.

1. **Small form factor**
   The board will be designed with SMT components. 0805 packages will be used for passive components when possible. Components may be placed on both sides of the board, but IC packages will only be placed on one side so that they can be skillet-reflowed and passive components can then be soldered manually on the opposite side.

2. **Tolerant to slip-ring induced noise in power lines**
   The board will have an on-board voltage regulator and large filtering capacitor before the regulator. The board will use 5V logic and be powered from 12V (supply voltage to RAMBo board), thus enabling significant energy storage in the filtering capacitor and preventing brown outs during power supply intermittence. The ground will be both run through a slip ring channel but also connected through the frame of the 3D printer. This way, intermittences in the slip ring are less likely to result in a floating ground.

3. **Minimum 1 channel ADC, ideally more to optionally provide redundant thermistors**
   The ADC selected has 4 (single ended) analog inputs.

4. **Digital serial output that is robust to slip-ring induced noise**
   The ADC selected has I^2C output. I^2C devices use pull up resistors and open collector pins to pull the data and clock lines low. Using pull up resistors on both sides of the slip ring will prevent the lines from ever floating. Low-pass filtering capacitors will also be added on both sides of the slip ring to prevent false clock and data transitions from slip ring intermittence.

5. **Serial digital output which is compatible with serial protocols already available on Rambo control board**
   I^2C is already implemented on the RAMBo board and can be implemented using a hardware peripheral module on the ATMega2560 – thus minimizing the programming overhead.

6. **Parts are affordable and obtainable**
   The ADC IC selected is in production and easily and cheaply (<$10) available through both suppliers (Digikey) and sample programs. The other components required are all widely available and standard form factors will be used.

Conceptual Circuit Design

As per standard practice, the resistance of the thermistor will be determined using a voltage divider with the thermistor forming the lower leg of the divider. Since the chassis will be grounded, placing the thermistor on the lower leg prevents the possibility of a short circuit in the scenario that a lead breaks and thermistor wire contacts the chassis (not uncommon in 3D printers). A diagram of the thermistor connection is shown in Figure 1.

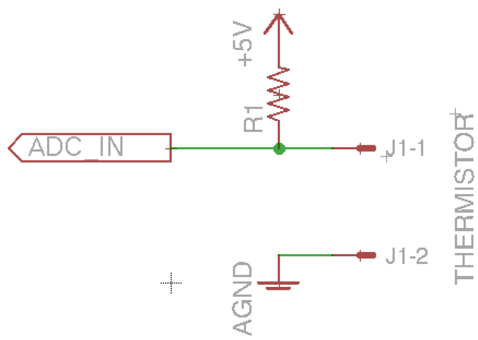


Figure 1: Thermistor Connection

The sizing of R1 is critical to achieving good temperature sensitivity in the required operating range. The operating temperature of 3D printer nozzles is typically between 180°C (PLA plastic) to 220°C (ABS plastic), thus temperature sensitivity should be maximized ~200°C. The thermistor used will be the same as the original 3D printer, an EPCOS B57560G1104 which has a nominal resistance of 100k at 25°C. The parameters necessary to calculate the Steinhart-hart coefficients are shown in Figure 2.

Electrical specification and ordering codes

R_{25} Ω	No. of R/T characteristic	$B_{25/85}$ K	$B_{0/100}$ K	$B_{25/100}$ K	Ordering code
2 k	8401	3420	3390 ±1%	3436	B57560G0202+000
2 k	8401	3420	3390 ±1%	3436	B57560G0202+002
5 k	8402	3480	3450 ±1%	3497	B57560G0502+000
5 k	8402	3480	3450 ±1%	3497	B57560G0502+002
10 k	7003	3612	3586	3625 ±1%	B57560G1103+005
10 k	7003	3612	3586	3625 ±1%	B57560G1103+007
10 k	8307	3478	3450	3492 ±1%	B57560G1103+000
10 k	8307	3478	3450	3492 ±1%	B57560G1103+002
20 k	8415	3992	3970 ±1%	4006	B57560G0203+000
20 k	8415	3992	3970 ±1%	4006	B57560G0203+002
30 k	7002	3973	3944	3988 ±1%	B57560G1303+005
30 k	7002	3973	3944	3988 ±1%	B57560G1303+007
50 k	8403	3992	3970 ±1%	4006	B57560G0503+000
50 k	8403	3992	3970 ±1%	4006	B57560G0503+002
100 k	8304	4072	4036	4092 ±1%	B57560G1104+000
100 k	8304	4072	4036	4092 ±1%	B57560G1104+002
1400 k	8406	4557	5133 ±2%1)	4581	B57560G0145+000
1400 k	8406	4557	5133 ±2%1)	4581	B57560G0145+002

+ = Resistance tolerance
F = ±1%
G = ±2%
H = ±3%

Figure 2: EPCOS 100k thermistor data

To determine the optimum value of R1, an excel template for calculating the ADC value and sensitivity was created. To accurately calculate the sensitivity, the ADC's input impedance and PGA setting must also be considered. The input impedance for the selected ADC (as a function of PGA setting, as indicated by full scale voltage), is shown in Figure 3.

FS (V)	DIFFERENTIAL INPUT IMPEDANCE
±6.144V(1)	22MΩ
±4.096V(1)	15MΩ
±2.048V	4.9MΩ
±1.024V	2.4MΩ
±0.512V	710kΩ
±0.256V	710kΩ

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

Figure 3: ADC Input impedance as a function of PGA setting (indicated by full scale voltage)

A list of available PGA settings is shown in Figure 4: PGA Gain Settings and Full Scale Voltages

PGA SETTING	FS (V)
2/3	±6.144V(1)
1	±4.096V(1)
2	±2.048V
4	±1.024V
8	±0.512V
16	±0.256V

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

Figure 4: PGA Gain Settings and Full Scale Voltages

To approximate the thermistor resistance as a function the Steinhart-Hart equation was used. In the physical implementation a look-up table will be used for better accuracy, but for approximating sensitivity the Steinhart-Hart model will be sufficient. For a given β parameter and corresponding temperatures, the Steinhart-Hart equation can be rearrange to solve for the thermistor resistance.

$$R_2 = \frac{R_1}{exp\left(\beta_{T1/_{T2}}\left({}^1/_{T_1} - {}^1/_{T_2}\right)\right)} \qquad [1]$$

Since our system will be operating >100°C, the $\beta_{25/_{100}}$ parameter shown in Figure 2 was used.

The calculated thermistor resistance and sensitivity is shown in Figure 5.

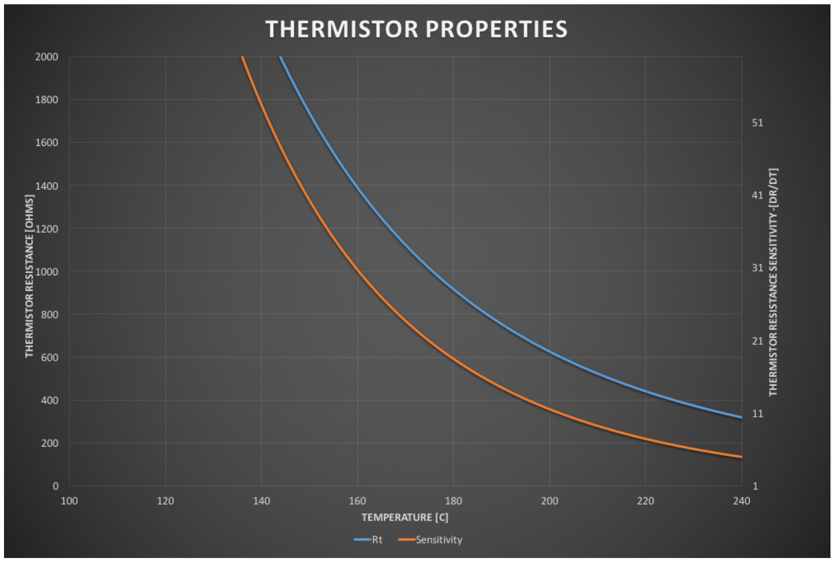


Figure 5: Resistance and Sensitivity Curves for EPCOS 100K Thermistor

Based on experimentation with the excel template, a fixed resistance (R1) of 10K ohms and PGA setting of 4 was chosen. Based on this resistance and the ADC input impedance, the voltage shown in Figure 6 is produced at the ADC input.

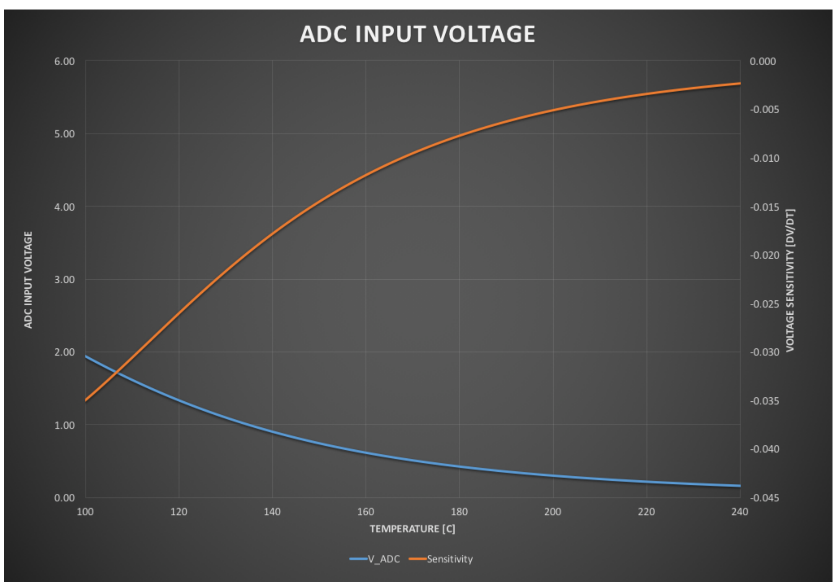


Figure 6: ADC Input Voltage and Sensitivity

With the parameters listed above, the following ADC reading curve is generated for the 12-bit ADC. The selected parameters produce ~85% of the maximum ADC sensitivity at 200°C, corresponding to a temperature resolution of 0.4°C. Note that the ADC saturates below ~125°C. If lower temperature readings are required, the ADC gain can be adjusted in real time. A plot of the ADC reading for a gain setting of 2/3 is shown in Figure 8.

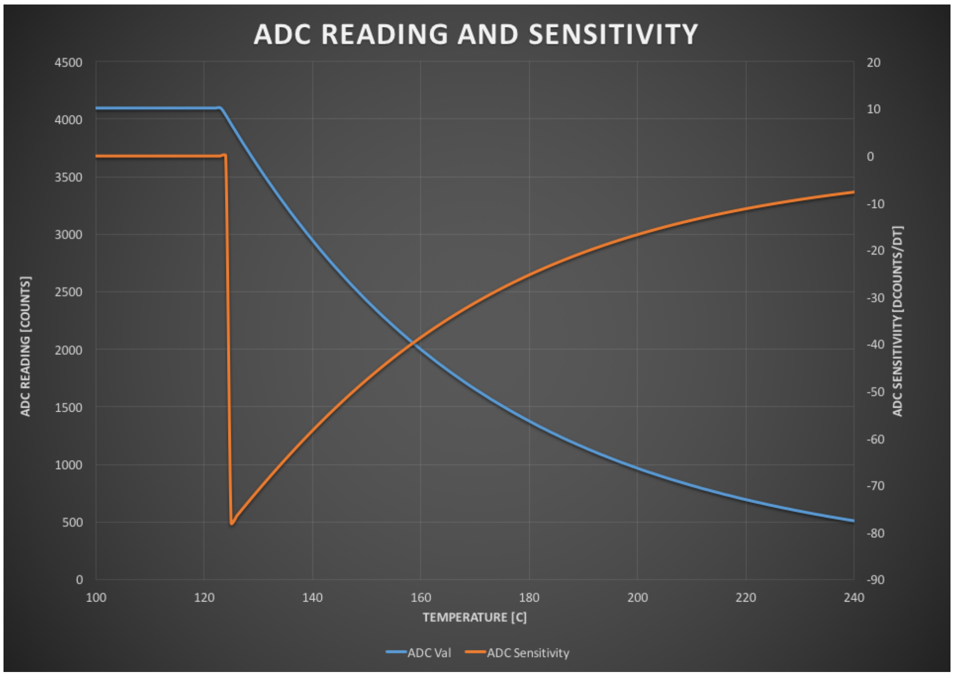


Figure 7: ADC Reading and Sensitivity with a PGA gain of 4. Note saturation at ~125℃.

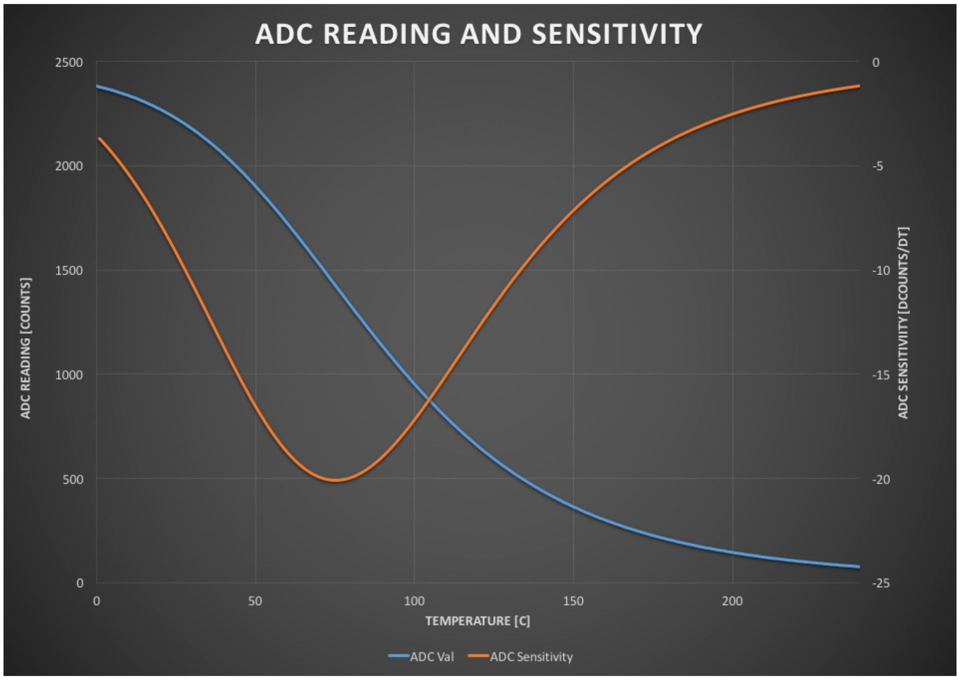


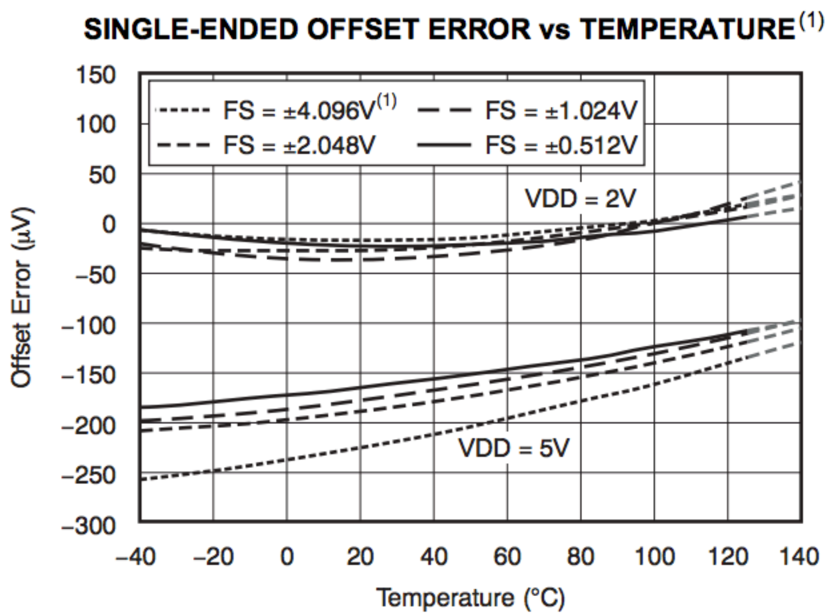
Figure 8: ADC Reading and Sensitivity with a PGA gain of 2/3. Note that the signal does not saturate above 0℃.

Component Requirements/Selection

ADC

Since the ADC is the main component in the design it has been selected. The ADC selected is the Texas Instrument's ADS1015. It is a 4 channel I^2C 12-bit delta-sigma ADC with built in programmable gain amplifier (PGA). As discussed above, the PGA will enable tuning of the circuit to maximize the thermistor sensitivity in the temperature range the nozzle will be operating in.

Since the board will be mounted near the heated extruder nozzle operating temperature and vibrational sensitivity is a concern. The ADS1015 is qualified for use in automotive applications and thus should be robust to both high temperatures and vibrations. Additionally, the ADC has a offset error minimum at the temperature range we expect the board to be at (~60-80C).



The ADS1015 has a VSSOP-10 package which can be soldered using solder paste and a reflow skillet. The small package and low lead count will help to keep the overall board size small.

Voltage Regulator

The exact voltage regulator has not been selected at this time but requirements have been defined and there exists many options that will meet the requirements. Because the regulator will be providing power to an ADC and the positive leg of the thermistor voltage divider a linear regulator should be used to provide the most stable voltage. Drop out voltage is not a consideration since the power supply (12v) is more than twice the supply voltage. Although there is a significant voltage drop across the regulator, current draw due to the ADC is extremely low. Thus it is not likely that heat dissipation will be an issue. An approximation of the ADC current draw is shown in Figure 9. Even at worse case scenario (ADC draw 250uA), the

ADC power dissipation is only 1.25mW, and a typical linear regulator would only dissipate 1.75mW. These dissipations will increase slightly due to the current draw of the thermistor voltage divider and I^2C pull up resistors, but will still be at least an order of magnitude below the maximum heat dissipation capabilities for most regulator packages.

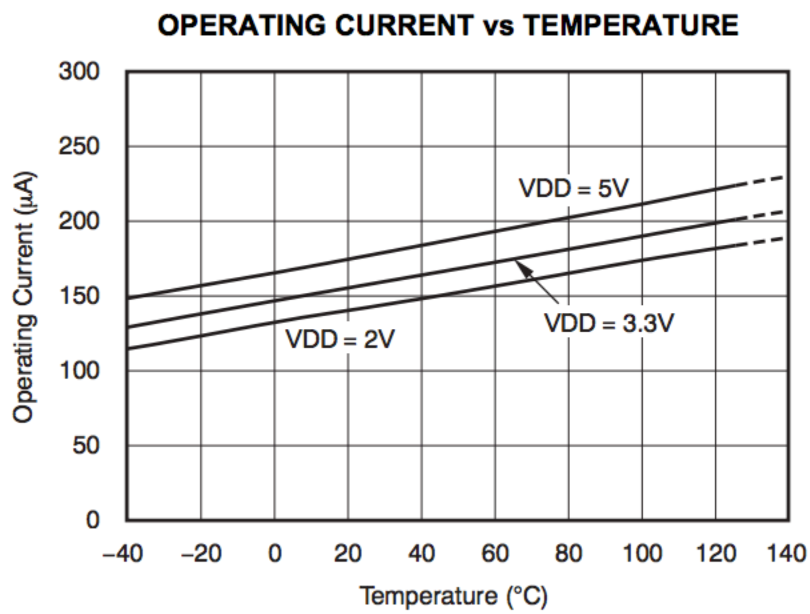


Figure 9: ADC Current Draw

Filtering and protection

To filter the input and provide power during slip ring intermittence a ~100uF capacitor should be connected across the input terminals. Since slip ring intermittence could potentially cause high speed voltage transients, which could induce flyback voltages in the power leads running to the board, it is important to also include a Zener diode between the power inputs. This will also provide reverse voltage protection as long as the the power supply is current is not to high to damage the Zener. Fuses will not be included since all currents should be extremely low and board real estate is a premium.

To help eliminate slip-ring induced transients on the clock and data line, each line will use a bypass capacitor. The value for this capacitor will be sized to minimally attenuate the I^2C clock frequency (400kHz) but suppress higher frequency transients. As previously mentioned, I^2C pull up resistors will be included on both sides of the slip ring to prevent line floating.

A schematic diagram of the filtering and protection on both sides of the slip ring is shown in Figure 10.

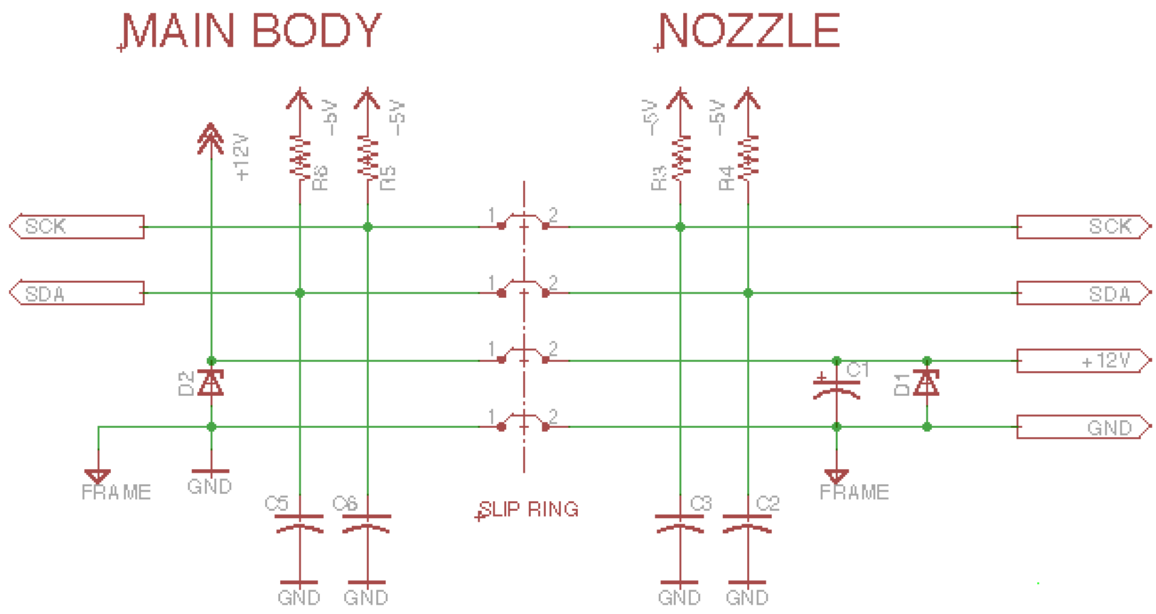


Figure 10: Schematic of filtering and protection for slip-ring induced voltage transients

References

TEXAS INSTRUMENTS. DATASHEET: *ULTRA-SMALL LOW-POWER 12-BIT ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE.*
Retrieved from http://www.ti.com/lit/ds/symlink/ads1015-q1.pdf.

TDK. DATASHEET: *NTC Thermistors for Temperature Measurement.*
Retrieved from en.tdk.eu/inf/50/db/.../Glass_enc_Sensors__B57560__G560__G1560.pdf.