Carnegie Mellon University

16-681A

MRSD Project I

Individual Lab Report 05
Team C: COBORG

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Sponsor:
Biorobotics Lab

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1 Individual Progress

We received our PCB so I have been working to build that up and test the functionality. I helped Husam solder all of the components to the board. Once everything was soldered on, I conducted gradual testing to ensure nothing would be damaged once powered. I did resistance testing between power and ground at each input and output port to ensure there were no short-circuits. I verified resistance values at each resistor and verified the voltage drops across each diode. I checked continuity between pins connected on the schematic to ensure nodes of the circuit were properly soldered to each other. Once all of these pre-checks were passed, I plugged in power to both of the input sources. I confirmed that the related LEDs were illuminated, and that the voltage of the output ports was what was expected. All LEDs were successfully illuminated for both input ports and the outputs for the motors (36VDC out) and computer (19.5VDC out), but not for the logic output (5VDC out). I found a problem with the 5VDC voltage regulator that will be further discussed in the challenges section. The output voltage for the motor output was as expected at roughly 36VDC, but the output for the computer was slightly higher than desired at 20.5VDC as opposed to the expected 19.5VDC. This issue will also be further discussed in the challenge section. We ordered an AC/DC converter that outputs to 36VDC, so I built up a cable to tie a wall outlet to the input AC pins of the converter. I then tested the functionality of the board with the external power and battery power sources by plugging the power sources into their respective sources and confirmed proper output voltages at the output pins, as seen in Figure 1 below. I tested the circuit has successful uninterrupted power with varied supply by unplugging each input power supply and re-confirming proper output voltages. Once these tests were successful, we integrated the board with the CoBorg system. We plugged in the external supply and the battery to the input ports and connected the output ports to the CoBorg motors and the Zotac computer. Everything successfully powered up and remained powered through unplugging the external power supply without any power interruption, proving proper function of the circuit.

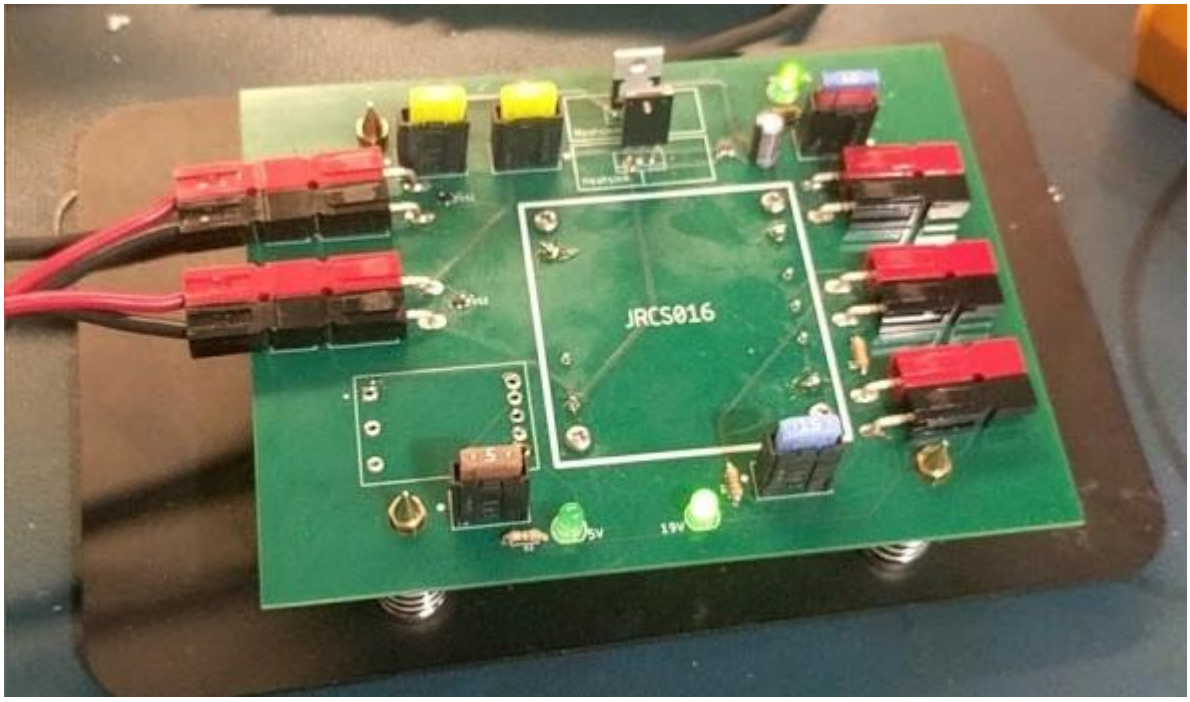

Figure 1. CoBorg Power Distribution PCB Buildup

For the voice subsystem, I worked with Jonathan to make the edits to the validation plan and finalize for the SVD demo. We established the concept of an “irritation failure” according to Dr. Dolan’s comments during Progress Review 3. An irritation failure occurs when it takes more than 2 tries to recognize the trigger word “CoBorg” or when there is a false positive trigger on the “CoBorg” keyword. We ran through a couple trials of the validation plan, then planned to run 50+ trials to establish a full dataset of validation points to ensure confirmation of requirements. For the SVD, we plan to only run through this plan 2-3 times as a proof of concept.

2 Challenges

The process of building up the PCB went smoothly but testing revealed some problems that needed fixing. First, the 5VDC regulator was unresponsive to the input power and did not produce anything at it’s output pins. After some testing and analysis, we realized that we accidentally ordered the regulator with negative enable logic requiring an enable circuit that we did not have on the PCB. The fix was rather simple as we just needed to order a different regulator within the same family with positive enable logic so that it will work in our circuit. Luckily, this regulator issue was isolated to the 5VDC logic output which was mostly developed as a “just in case” functionality so we could proceed with functionality and integration testing without it. We have since received the new part and will be installing it on the board this weekend. The second issue we ran into was that the output for the computer was slightly higher than the desired value of 19.5VDC at 20.5VDC. This was caused by tolerancing in the trim resistor bringing it from the rated 33.3kΩ to 32.4kΩ and tolerances within the regulator itself causing slight skewing from the listed output equation is $R_{trim} = \frac{700-(10*V_{out})}{(V_{out}-4)} k\Omega$. To fix this issue, we tested different trim resistors with slightly increasing resistances and measured the output voltage. Running into this issue now was a blessing in disguise as we are planning to switch computers to the Jetson Xavier and the Jetson Xavier is rated for input voltage only up to 19VDC as opposed to the 19.5VDC we had originally designed for the Zotac computer. So we settled on a trim resistor around 37kΩ bringing the computer output voltage to measure to roughly 18.7VDC.

3 Teamwork

Feng Xiang has continued to focus on the actuated manipulation subsystem. He calibrated the URDF model to the actual CoBorg arm to fix that contribution to the inaccuracies of position control of the CoBorg arm. With this fix, he measured the transform between the robot and camera frames to ensure the improved accuracy. Then the actuated manipulation was ready for pre-SVD validation test runs with Jonathan's validation plan, so they ran some trials. Now that the actuated subsystem is ready for validation to our SVD standards, Jonathan and Feng started working on implementing impedance control for safe manipulation around a human user. So far this has created more problems than solutions, but we have talked to our advisor Julian and Professor Kroemer for advice and have some ideas to move forward. From here, Feng is going to focus on optimizing the actuated manipulation subsystem for the SVD by improving the speed of the planning node and writing scripts to make the SVD demo more seamless.

Jonathan, along with the work he has done with Feng on the actuated manipulation subsystem, has been working with everyone to develop and flesh out the validation plans. He has worked with each subsystem technical lead to run through the drafts of the validation plans and has updated the plans according to the lead's recommendations and trial test results. From here, he will finalize the validation plan for SVD and perform statistical analysis on the more in-depth subsystem testing datapoints (external of SVD). He will also continue to assist Feng with the actuated manipulation subsystem implementing the impedance control and other path planning strategies. He will also continue to ensure success integration of systems via managing the ROS framework.

Yuqing finalized the vision subsystem and validated the performance according to the established validation plan. With the finalized vision subsystem, she has worked with Jonathan to run the SVD test for the vision subsystem, she has generated data points corresponding to the accuracies relation to the ground truth of the system, and has begun integrating the vision subsystem with the actuated manipulation subsystem. From here, Yuqing is going to continue SVD rehearsal and make any tuning adjustments necessary to ensure SVD success. Next is to continue integration of the vision subsystem with the actuated manipulation subsystem.

Husam worked with me to build up the CoBorg power distribution PCB. He handled most of the soldering of the components to the board. He also handled all of the ordering and part procurement needed for the PCB. He plans to develop a timing service within our ROS framework so that we can validate our time-based requirements. He also plans to work on the actuated manipulation subsystem by developing an action server to interface with Move-It.

4 Plans

With our subsystems fully developed to our promised SVD presentation standards, we are focusing on validation plan that we will show parts of for SVD. We will be running through this as a team to make sure we can fit the full demo in the allotted time and to ensure all kinks are worked out of the subsystems. Parallelly, we will be running the individual subsystem's validation plans to establish validation data. For the voice subsystem, this will entail running through the full aforementioned voice validation plan 50+ times to ensure sufficient data points. From there, we will run statistical analysis on the validation data to confirm that the subsystem requirements have been met.

Additionally, to prepare for the PCB demonstration before SVD, I would like to further test the PCB performance. We have already tested and confirmed the functionality of the PCB integrated with the CoBorg, but to confirm that the power is successfully switching, I need to place ammeters in line with each power supply to see how much power is being drawn from each source under different power conditions. Overall, the PCB already works well so the next step will be integrating it onto the CoBorg using the mounting bracket.